



Stretchable and Foldable Silicon Integrated Circuits

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Science **320**, 507 (2008);
DOI: 10.1126/science.1154367

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stretch force reduction due to nanotube meandering. This structure provides a volume per strut of $D'L^2 \sin(120^\circ)$ and a calculated density of $\rho_{\text{calc}} = W_L/[D'L \sin(120^\circ)]$, where W_L is the strut weight per unit length and D' is the sum of the covalent diameter of the nanotube and the 0.34-nm van der Waals diameter of carbon (δ). By equating calculated sheet densities to the observed sheet densities, interjunction lengths of 54.3 nm and 39.5 nm are calculated for the MWNT and SWNT sheets, respectively. Although these distances seem shorter than suggested by the micrographs of Fig. 2, note that the micrographs are for the sheet surface (the face originally in contact with the filter membrane) and do not provide the junction density and corresponding L in the buckypaper interior.

To predict the Poisson's ratio of buckypaper, we calculate the elongation force constant $k_{\text{SB}}(\delta)$ from the observed Young's modulus Y according to $k_{\text{SB}} = 2D'Y \sin(120^\circ)/(1 - \nu_1)$. Although this little affects the results, ν_1 in this equation is the self-consistently calculated value instead of the measured value. The k_{B} for the MWNTs is the sum of bending force constants for all component SWNTs nested within the MWNTs, and the k_{B} for SWNT bundles is derived from the measured average Young's modulus for bending (Y_{B}) 20-nm-diameter SWNT bundles (50 GPa) (29), using the force constant for bending a solid cylindrical rod, $k_{\text{B}} = 3\pi R^4 Y_{\text{B}}/(4L^3)$ (26). The predicted Poisson's ratios are -0.17 for MWNT buckypaper (versus the observed -0.20) and 0.17 for SWNT buckypaper (versus the observed 0.06). Increasing Y_{B} to 81 GPa decreases the calculated ν_1 for SWNT buckypaper to the observed value, and this Y_{B} is within the range of experimental uncertainty for Y_{B} (29).

These results indicate that large negative Poisson's ratios can be achieved by using large-diameter MWNTs having as many interior walls as possible. Although all nanotube walls contribute additively to k_{B} , only the outer wall contributes to k_{SB} unless the MWNTs are extremely long. Likewise, decreasing the separation between effectively welded inter-nanotube contacts (such as by increasing sheet density) can decrease Poisson's ratio. However, the effects of these structure changes are not simple, because increasing k_{B} and decreasing L can decrease nanotube meandering between junctions, and this decrease of meandering can provide a positive contribution to k_{SB} .

Negative Poisson's ratios are sometimes accompanied by much rarer mechanical properties: negative linear compressibilities and negative area compressibility—meaning that a material expands in either one or two orthogonal directions when hydrostatic pressure is applied (I). A negative linear compressibility is the inverse of another strange property, increasing density when elongated in a direction where linear compressibility is negative, and both require that $1 - \nu_1 - \nu_3 < 0$. Using the above equations for ν_1 and ν_3 as a function of R and γ for the model of Fig. 1C, negative in-plane compressibility (Fig. 1D), negative area compressibility for the sheet plane, and stretch densification are predicted for $\cos \gamma >$

$(2/3)^{1/2}$, which implies $\gamma < 35.3^\circ$. However, the average γ needed for achieving these properties will decrease as a result of in-plane nanofiber meandering, because only the tensile strain component resulting in thickness change affects ν_3 .

The observed continuous tunability of Poisson's ratio, modulus, strength, toughness, density, and electrical conductivity of nanotube sheets could be useful for applications, as could mechanical property optimization using mixtures of nanotubes. However, the change of Poisson's ratio from positive to negative is especially interesting and unexpected. This tunability, which we can now explain, could be exploited in the design of sheet-derived composites, artificial muscles, gaskets, stress/strain sensors, and chemical sensors where analyte absorption induces mechanical stresses. Even shaping processes are affected, because bending a thick nanotube sheet strip will result in either convex or concave lateral deformation (Fig. 1A, inset), depending on the sign of the in-plane Poisson's ratio.

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- The simplest model that provides these key features of the nanotube sheets has hexagonal space group $P6_22$ and inter-nanotube noncovalent junctions located at $(0.5, 0, 0)$ and equivalent locations in the unit cell. The same mechanical properties result for the intimately related structure in Fig. 1C, in which each successive layer of zigzag chains is equally likely to be added in either of two possible directions.
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- We thank R. Raj, S. Shaw, R. Hou, and J. Levinson for their contributions; J. Belew for the micrograph of Fig. 2C; and C. A. Bronkhorst for permission to use the micrograph of Fig. 2A. Supported by NSF grant DMI-0609115, Air Force Office of Scientific Research grant FA9550-05-C-0088, Lintec Corporation, and the Brazilian agencies Fundação de Amparo à Pesquisa do Estado de São Paulo and Conselho Nacional de Pesquisas Científicas.

Supporting Online Material

www.sciencemag.org/cgi/content/full/320/5875/504/DC1
Materials and Methods
SOM Text
Figs. S1 and S2
References

28 August 2007; accepted 20 March 2008
10.1126/science.1149815

Stretchable and Foldable Silicon Integrated Circuits

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We have developed a simple approach to high-performance, stretchable, and foldable integrated circuits. The systems integrate inorganic electronic materials, including aligned arrays of nanoribbons of single crystalline silicon, with ultrathin plastic and elastomeric substrates. The designs combine multilayer neutral mechanical plane layouts and “wavy” structural configurations in silicon complementary logic gates, ring oscillators, and differential amplifiers. We performed three-dimensional analytical and computational modeling of the mechanics and the electronic behaviors of these integrated circuits. Collectively, the results represent routes to devices, such as personal health monitors and other biomedical devices, that require extreme mechanical deformations during installation/use and electronic properties approaching those of conventional systems built on brittle semiconductor wafers.

Realization of electronics with performance equal to established technologies that use rigid semiconductor wafers, but in lightweight, foldable, and stretchable formats would enable many new applications. Examples include

wearable systems for personal health monitoring and therapeutics, “smart” surgical gloves with integrated electronics, and electronic eye-type imagers that incorporate focal plane arrays on hemispherical substrates ($I-3$). Circuits that use

organic (4, 5) or certain classes of inorganic (6–13) electronic materials on plastic or steel foil substrates can provide some degree of mechanical flexibility, but they cannot be folded or stretched. Also, with few exceptions (11–13) such systems offer only modest electrical performance. Stretchable metal interconnects with rigid (14) or stretchable (15–17) inorganic device components represent alternative strategies that can also, in certain cases, provide high performance. In their existing forms, however, none of these approaches allows scaling to circuit systems with practically useful levels of functionality.

We present routes to high-performance, single-crystalline silicon complementary metal-oxide semiconductor (Si-CMOS) integrated circuits (ICs) that are reversibly foldable and stretchable. These systems combine high-quality electronic materials, such as aligned arrays of silicon nanoribbons, with ultrathin and elastomeric substrates, in multilayer neutral mechanical plane designs and with “wavy” structural layouts. High-performance n- and p-channel metal-oxide semiconductor field-effect transistors (MOSFETs), CMOS logic gates, ring oscillators, and differential amplifiers, all with electrical properties as good as analogous systems built on conventional silicon-on-insulator (SOI) wafers, demonstrate the concepts. Analytical and finite element method (FEM) simulation of the mechanics, together with circuit simulations, reveal the key physics. We implement single-crystalline silicon because it provides excellent electronic properties, including high electron and hole mobilities. Commodity bulk silicon wafers (18), for cost-sensitive applications, or SOI wafers provide the source of the ultrathin pieces of Si that are required. Vacuum-evaporated materials such as nanocrystalline Si (19), which also enable high performance, might offer further advantages in cost. The same approaches to stretchable and foldable integrated circuits reported here can be used with these and other related classes of materials. The strategies reported here are important not only for the Si-CMOS circuits that they enable but also for their straightforward scalability to much more highly integrated systems with other diverse classes of electronic materials whose intrinsic brittle, fragile

mechanical properties would otherwise preclude their use in such applications.

Figure 1A schematically summarizes the key steps for forming ultrathin, foldable, and stretchable circuits and presents optical images of representative systems at different stages of the process. The procedure begins with spin-casting a sacrificial layer of poly(methylmethacrylate) (PMMA) (~100 nm) followed by a thin, substrate layer of polyimide (PI) (~1.2 μm) on a Si wafer that serves as a temporary carrier (see supporting online material). A transfer printing process with a poly(dimethylsiloxane) (PDMS) stamp (20, 21) delivers to the surface of the PI organized arrays of n- and p-doped Si nanoribbons (Fig. 1B, inset) with integrated contacts, separately formed from n-type source wafers. Automated stages specially designed for this printing enable multilayer registration with ~2 μm accuracy (12). Depositing and patterning SiO₂ (~50 nm) for gate dielectrics and interconnect crossovers, and Cr/Au (5/145 nm) for source, drain, and gate electrodes and interconnects yield fully integrated Si-CMOS circuits with performance comparable to similar systems formed on SOI wafers (fig. S1). Figure 1C shows an image of an array of Si-CMOS inverters and isolated n- and p-channel MOSFETs (n-MOSFETs and p-MOSFETs, respectively) formed in this manner, still on the carrier substrate. In the next step, reactive ion etching forms a square array of small holes (~50 μm diameters, separated by 800 μm) that extend through the

nonfunctional regions of the circuits and the thin PI layer into the underlying PMMA by flow of solvent through the etch holes to release ultrathin, flexible circuits in a manner that does not degrade the properties of the devices. These systems can be implemented as flexible, free-standing sheets, or they can be integrated in wavy layouts on elastomeric substrates to provide fully reversible stretchability/compressibility (Fig. 1A). The schematic cross-sectional view at the bottom right illustrates the various layers of this Si-CMOS/PI system (total thickness ~1.7 μm). The ultrathin circuits exhibit extreme levels of bendability, as illustrated in Fig. 1C, without compromising the electronic properties (fig. S2). There are two primary reasons for this behavior. The first derives from elementary bending mechanics in thin films, where the surface strains are determined by the film thickness, t , divided by twice the radius of curvature associated with the bending, r (22). Films with $t = 1.7$ μm can be bent to r as small as ~85 μm before the surface strains reach a typical fracture strain (~1% in tension) for the classes of high-performance inorganic electronic materials used here. A second and more subtle feature emerges from full analysis of the bending mechanics in the material stacks of the circuits. The results indicate that the neutral mechanical plane, which defines the position through the thickness of the structure where strains are zero for arbitrarily small r , lies in

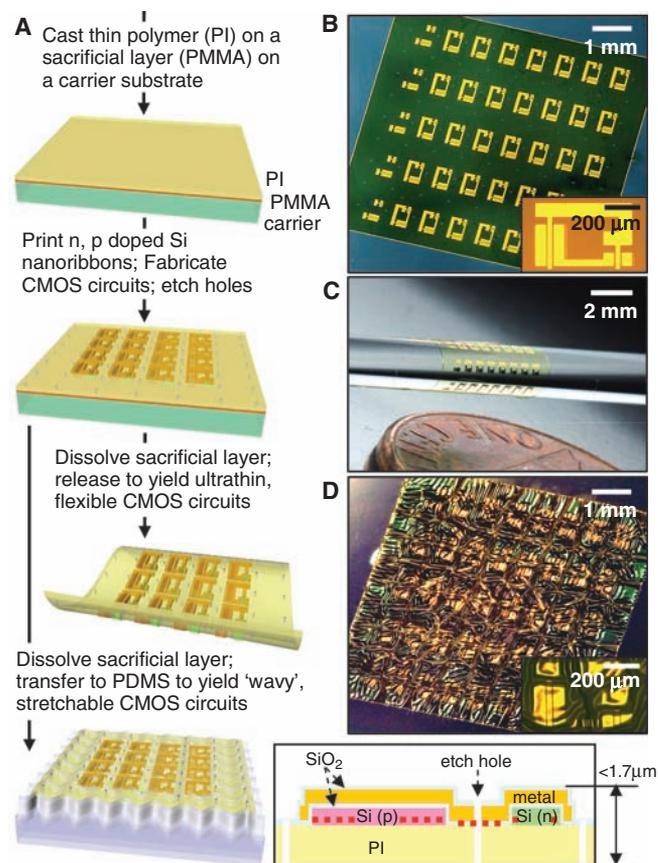


Fig. 1. (A) Overview of the fabrication process for ultrathin CMOS circuits that exploit silicon nanoribbons and enable extreme levels of bendability (third frame from the top) or fully reversible stretchability/compressibility (bottom frame on the left) and schematic cross-sectional view with neutral mechanical plane indicated with a red dashed line (bottom frame on the right). (B to D) Optical images of circuits on the carrier wafer and magnified views of a single CMOS inverter (inset) (B), on a thin rod after removal from this carrier (C), and in a wavy configuration on PDMS (D).

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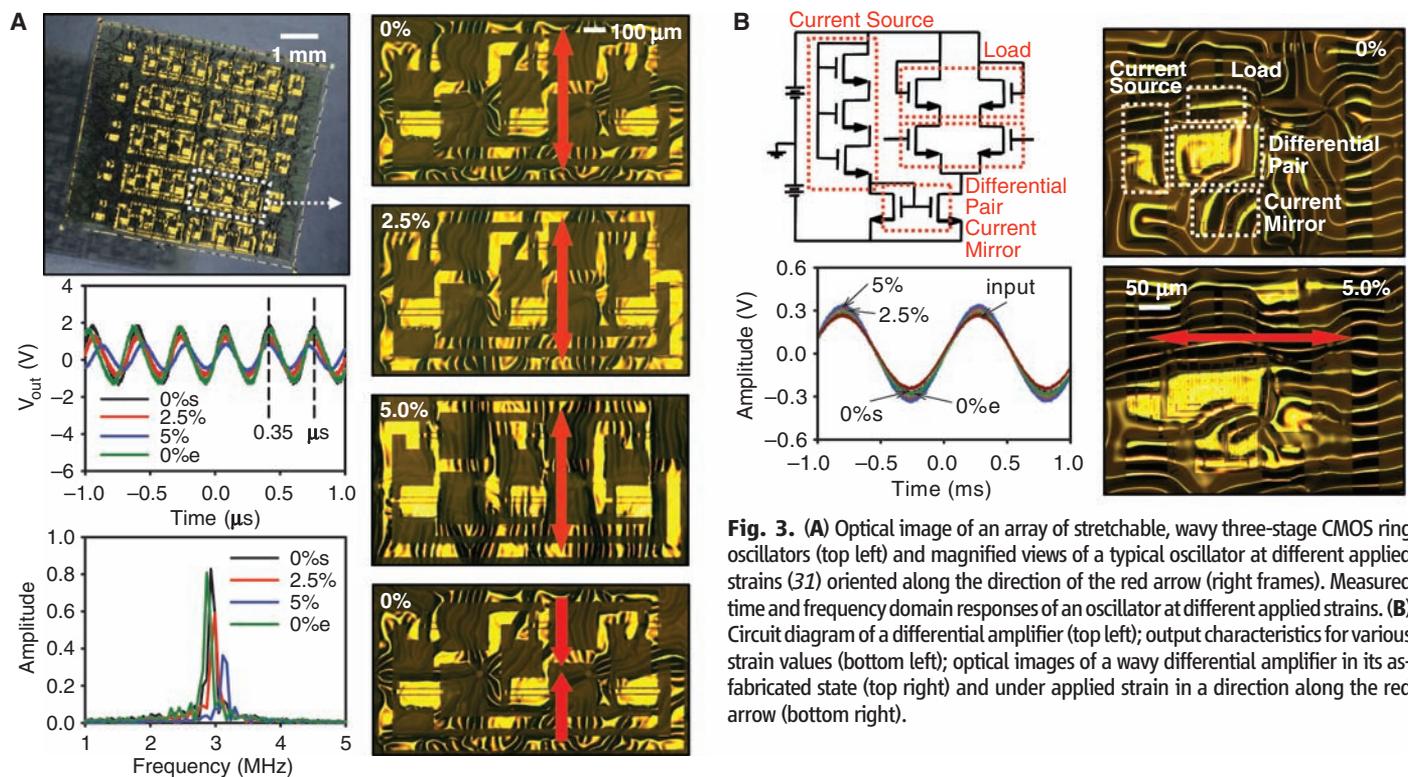
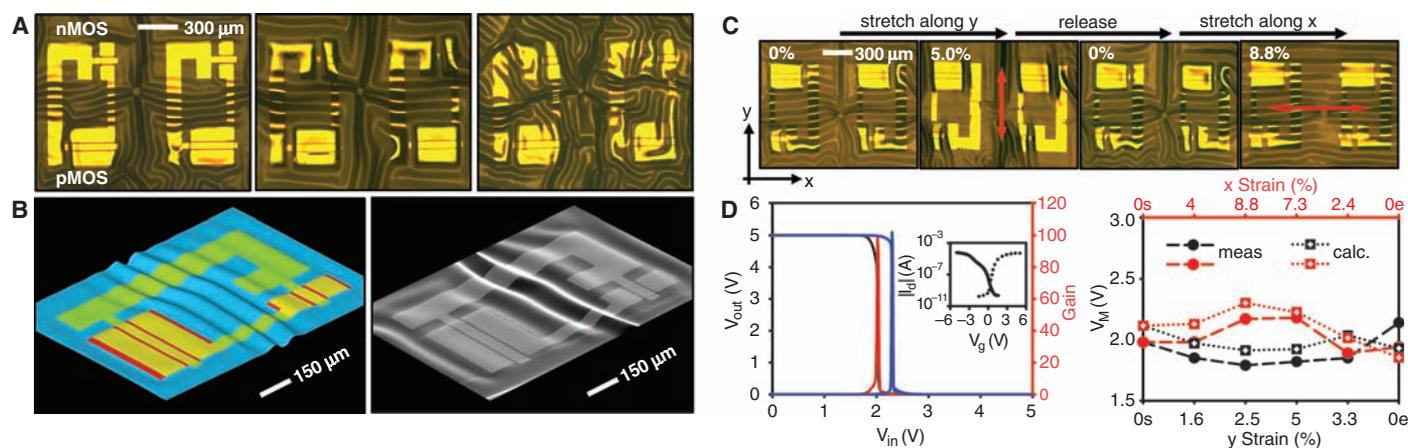
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the electronic device layers (fig. S3). In other words, the high moduli of the electronic materials move the neutral mechanical plane from the geometric midplane, which lies in the PI, to the device layers. The illustration at the bottom right of Fig. 1 indicates with dashed red lines the approximate locations of this neutral mechanical plane in different regions of the system. This situation is highly favorable because the fracture strains of the materials used in the circuits are substantially lower than those for fracture or plastic deformation in the PI ($\sim 7\%$). Two

disadvantages of such circuits are their lack of stretchability and, for certain applications, their low flexural rigidity. These limitations can be circumvented by implementing extensions of concepts that achieve stretchable, wavy configurations of sheets and ribbons of silicon and gallium arsenide (*15, 16*), in a procedure illustrated in the bottom frame of Fig. 1A. The fabrication begins with removal of the ultrathin circuits from the carrier substrate using a PDMS stamp, evaporating a thin layer of Cr/SiO₂ (3/30 nm) onto the exposed PI surface (i.e., the surface that was in

contact with the PMMA), and then generating $-OH$ groups on the surfaces of the SiO₂ and a biaxially prestrained PDMS substrate ($\epsilon_{pre} = \epsilon_{xx} = \epsilon_{yy}$, where the x and y coordinates lie in the plane of the circuit) by exposure to ozone induced with an ultraviolet lamp. Transfer printing the circuit onto the PDMS substrate, followed by mild heating, creates covalent linkages to form strong mechanical bonding between the Si CMOS/PI/Cr/SiO₂ and the PDMS. Relaxing the prestrain induces compressive forces on the circuits that lead to the formation of complex wavy



patterns of relief by nonlinear buckling processes. The location of the neutral mechanical plane in the device layers, as noted previously, facilitates the nondestructive bending that is required to form these wavy patterns. Circuits in this geometry offer fully reversible stretchability/compressibility without substantial strains in the circuit materials themselves. Instead, the amplitudes and periods of the wave patterns change to accommodate applied strains (ϵ_{appl} , in any direction in the plane of the circuit), with physics similar to an accordion bellows (23). Figure 1D presents an optical image of a wavy Si-CMOS circuit on PDMS, formed with a biaxial prestrain of $\sim 5.7\%$. The thickness of the PDMS can be selected to achieve any desired level of flexural rigidity, without compromising stretchability.

The left, middle, and right frames of Fig. 2A show optical micrographs of wavy Si-CMOS inverters formed with $\epsilon_{\text{pre}} = 2.7\%$, 3.9% , and 5.7% , respectively. The wave structures have complex layouts associated with nonlinear buckling physics in a mechanically heterogeneous system. Three features are notable. First, the waves form most readily in the regions of smallest flexural rigidity: the interconnect lines between the p-MOSFET and n-MOSFET sides of the inverter and the electronically inactive parts of the circuit sheet. Second, as ϵ_{pre} increases, the wave structures begin to extend from these locations to all parts of the circuit, including the comparatively rigid device regions. Third, the etch holes, representative ones of which appear near the centers of these images, have a strong influence on the waves. In particular, waves tend to nucleate at these locations; they adopt wave vectors oriented tangential to the perimeters of the holes as a result of the traction-free edges at these locations. Cracks form, most commonly in the metal electrodes near the etch holes, when local strains rise to levels ~ 1 to 2% greater than the local prestrain. The maximum prestrain is $\sim 10\%$ (fig. S4); higher values lead to cracking upon release. The first two behaviors can be quantitatively captured using analytical treatments and FEM simulation, the third by FEM. Analysis

indicates, for example, that the p-MOSFET and n-MOSFET regions ($\text{SiO}_2/\text{metal}/\text{SiO}_2/\text{Si}/\text{PI}$, $\sim 0.05 \mu\text{m}/0.15 \mu\text{m}/0.05 \mu\text{m}/0.25 \mu\text{m}/1.2 \mu\text{m}$) adopt periods between 160 and $180 \mu\text{m}$ and that the metal interconnects ($\text{SiO}_2/\text{metal}/\text{SiO}_2/\text{PI}$, $\sim 0.05 \mu\text{m}/0.15 \mu\text{m}/0.05 \mu\text{m}/1.2 \mu\text{m}$) adopt periods between 90 and $110 \mu\text{m}$, all quantitatively consistent with experiment. Figure 2B shows the results of full, three-dimensional (3D) FEM modeling, together with a scanning electron micrograph of a sample. The correspondence is remarkably good, consistent with the deterministic, linear elastic response of these systems. (Slight differences are due to the sensitivity of the buckling patterns to the precise location and detailed shapes of the etch holes and some uncertainties in the mechanical properties of the various layers.) Both the analytics and the FEM indicate that for ϵ_{pre} up to 10% and $0\% < \epsilon_{\text{appl}} - \epsilon_{\text{pre}} < 10\%$, the material strains in the device layers remain below 0.4% and 1% , depending on the region of the circuit and the metal, respectively (fig. S4).

Figure 2, C and D, shows images and electrical measurements of inverters under different tensile, uniaxial applied strains, for a wavy circuit fabricated with $\epsilon_{\text{pre}} = 3.9\%$. As might be expected, the amplitudes and periods of waves that lie along the direction of applied force decrease and increase, respectively, to accommodate the resulting strains (fig. S5). The Poisson effect causes compression in the orthogonal direction, which leads to increases and decreases in the amplitudes and periods of waves with this orientation, respectively. Electrical measurements indicate that the Si-CMOS inverters work well throughout this range of applied strains. The left frame of Fig. 2D shows measured and simulated transfer curves, with an inset graph that presents the electrical properties of individual n-MOSFET and p-MOSFET devices with channel widths (W) of $300 \mu\text{m}$ and $100 \mu\text{m}$, respectively, to match current outputs, and channel lengths (L_c) of $13 \mu\text{m}$. These data indicate effective mobilities of $290 \text{ cm}^2/\text{Vs}$ and $140 \text{ cm}^2/\text{Vs}$ for the n- and p-channel devices, respectively; the on/off ratios in both cases are $>10^5$. The gains

exhibited by the inverters are as high as 100 at supply voltages (V_{DD}) of 5V , consistent with circuit simulations that use the individual transistor responses. The right frame of Fig. 2D summarizes the voltage at maximum gain (V_M) for different ϵ_{appl} along x and y . Tensile strains parallel to the transistor channels (i.e., along y) tend to reduce the compressive strains associated with the wavy structures in these locations (fig. S3). The complex, spatially varying strain distributions and the practical difficulties associated with probing the devices make simple explanations for the associated changes in electrical properties elusive. They also frustrate conclusive statements on the slightly different observed strain sensitivities of the p-channel and n-channel devices (fig. S5). Generally, we speculate that the overall tensile and compressive strains in these systems increase and decrease the electron mobility, respectively, with opposite effects on hole mobility (24–26), consistent with analysis of measured transistor data using standard long-channel MOS device models (27). Tensile strains in the x direction (i.e., perpendicular to the channels) cause opposite mechanical strains, due to the Poisson effect, and therefore also opposite changes in the electrical properties. At the level of the inverters, the changes in the transistors cause decreases and increases in V_M with parallel and perpendicular strains, respectively. Individual measurements of the transistors at these various strain states enable simulations of changes in the inverters (fig. S5); the results, also included in the right frame of Fig. 2D, are consistent with experiment. The devices also show good behavior under mechanical/thermal cycling (up to 30 cycles) (fig. S6).

More complex stretchable circuits can be fabricated using these inverters as building blocks. Figure 3A shows optical images, electrical measurements, and stretching tests on Si-CMOS ring oscillators that use three inverters identical to those in Fig. 2. The mechanical responses are qualitatively consistent with considerations described in the discussion of the inverters. The electrical measurements indicate stable oscillation frequencies of $\sim 3.0 \text{ MHz}$ at supply voltages of 10 V , even under severe buckling deformations and strains of 5% and larger. The measured frequencies were 2.9 MHz , 3.0 MHz , 3.1 MHz , and 2.9 MHz for 0% , 2.5% , 5% , and 0% applied strain, respectively. Formulating detailed explanations for these relatively small shifts is difficult, for reasons similar to those outlined in the discussion of the inverters. The expected strain-induced anisotropy in transport (28) must also be considered. More general classes of circuits are also possible. Figure 3B shows a differential amplifier (29) for a structural health monitor that integrates four components: a current source (three transistors with $L_c = 30 \mu\text{m}$ and $W = 80 \mu\text{m}$), a current mirror (two transistors with $L_c = 40 \mu\text{m}$, $W = 120 \mu\text{m}$; and $L_c = 20 \mu\text{m}$, $W = 120 \mu\text{m}$), a differential pair (two transistors with $L_c = 30 \mu\text{m}$ and $W = 180 \mu\text{m}$), and a load (two transistors

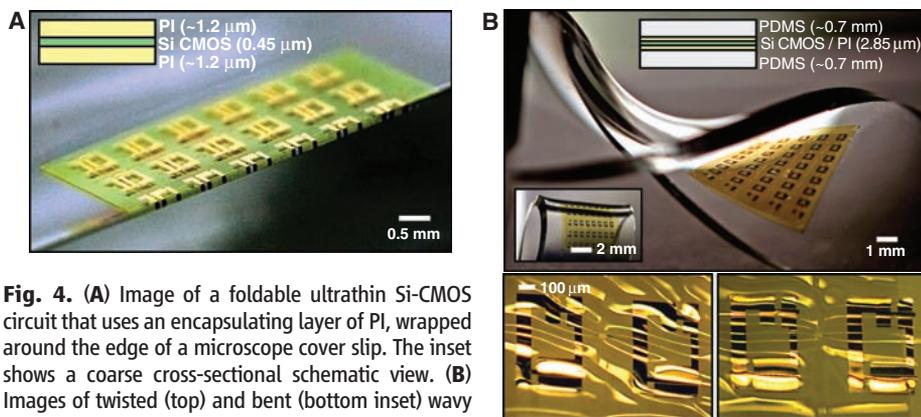


Fig. 4. (A) Image of a foldable ultrathin Si-CMOS circuit that uses an encapsulating layer of PI, wrapped around the edge of a microscope cover slip. The inset shows a coarse cross-sectional schematic view. (B) Images of twisted (top) and bent (bottom inset) wavy Si-CMOS circuit that uses a dual neutral plane design. The inset at the top shows a coarse cross-sectional view. Optical micrographs of inverters at the center (bottom left) and edge (bottom right) of the sample in the twisted configuration shown in the top frame.

with $L_c = 40 \mu\text{m}$ and $W = 80 \mu\text{m}$). The right frame shows an optical image of the corresponding wavy circuit (fig. S7). This amplifier is designed to provide a voltage gain of ~ 1.4 for a 500-mV peak-to-peak input signal. Measurements at various tensile strains along the red arrow show gains that vary by less than $\sim 20\%$: 1.01 without applied strain (0%, black), 1.14 at 2.5% strain (red), 1.19 at 5% strain (blue), and 1.08 after release (0%, green).

Although the ultrathin and wavy circuit designs described above provide unusually good mechanical properties, two additional optimizations can enable further improvements. Dominant failure modes observed at high applied strains ($\epsilon_{\text{appl}} - \epsilon_{\text{pre}} > \sim 10\%$) or degrees of bending ($r < \sim 0.05 \text{ mm}$) are caused by delamination of the device layers and/or fracture of the metal interconnects. A simple design modification that addresses these failures involves the deposition of an encapsulating layer on top of the completed circuits. Figure 4 illustrates a representative layout that includes a thin ($\sim 1.2 \mu\text{m}$) layer of PI on top of an ultrathin Si-CMOS/PI circuit. The resulting systems are extremely bendable, which we refer to as foldable, as demonstrated in the PI/Si-CMOS/PI circuit tightly wrapped over the edge of a microscope cover slip (thickness $\sim 100 \mu\text{m}$) in Fig. 4A. Even in this configuration, the inverters are operational and exhibit good electrical properties (fig. S8). Such foldability is enabled by the good adhesion of the PI layer and its encapsulation of the underlying layers preventing their delamination. Also, the PI layer shifts the metal interconnects at the neutral mechanical plane without moving this plane out of the silicon layers in other regions of the circuits (fig. S8). Such designs can also be incorporated in wavy configurations to enable stretchability/compressibility. The stretchable system presents, however, another challenge. As mentioned previously, the bendability of the Si-CMOS/PI/PDMS is influenced strongly by the thickness of the PDMS. Systems that are both stretchable and highly bendable require the use of thin PDMS. Relaxing the prestrain when using a thin PDMS substrate, however, results in an unwanted, overall bowing of the system rather than the formation of wavy circuit structures. This response occurs because of the very low bending stiffness of thin PDMS, which in turn results from the combined effects of its small thickness and extremely low modulus compared with the PI/Si-CMOS/PI. Neutral mechanical plane concepts that involve the addition of a compensating layer of PDMS on top of the PI/Si-CMOS/PI/PDMS system can avoid this problem. Figure 4B illustrates this type of fully optimized, dual neutral mechanical plane layout (i.e., PDMS/PI/Si-CMOS/PI/PDMS) and its ability to be stretched and bent. The optical micrographs at the bottom left and right of Fig. 4B illustrate the various configurations observed under extreme twisting and stretching of this system.

The strategies presented here demonstrate the degree to which extreme mechanical properties (i.e., stretchability and foldability) can be achieved in fully formed, high-performance integrated circuits by the use of optimized structural configurations and multilayer layouts, even with intrinsically brittle but high-performance inorganic electronic materials. In this approach, the desired mechanical properties are enabled by materials (e.g., PDMS, thin PI, and their multilayer assemblies) that do not need to provide any active electronic functionality. Such designs offer the possibility of direct integration of electronics with biological systems, medical prosthetics and monitoring devices, complex machine parts, or with mechanically rugged, lightweight packages for other devices. Further development of the mechanical concepts to provide, for example, expanded ranges of stretchability (30), to extend such electronic systems to other material types, and to exploit them in new classes of devices all appear to represent promising directions for future research.

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- Here, the tensile strains and applied strains are the global strains defined by the percentage change of substrate length.
- We thank T. Banks and K. Colvay for help with processing. The materials parts of this effort were supported by the U.S. Department of Energy (DoE), Division of Materials Sciences under award DE-FG02-07ER46471, through the Materials Research Laboratory (MRL). The general characterization facilities were provided through the MRL with support from the University of Illinois and from DoE grants DE-FG02-07ER46453 and DE-FG02-07ER46471. The mechanics theory and the transfer printing systems were developed under support from the Center for Nanoscale Chemical Electrical Mechanical Manufacturing Systems at the University of Illinois (funded by the NSF under grant DMI-0328162).

Supporting Online Material

www.sciencemag.org/cgi/content/full/1154367/DC1
Materials and Methods
Figs. S1 to S8

19 December 2007; accepted 10 March 2008
Published online 27 March 2008;
10.1126/science.1154367
Include this information when citing this paper.

Near-Field Plates: Subdiffraction Focusing with Patterned Surfaces

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Using a patterned, grating-like plate to control the electromagnetic near field, we demonstrate focusing well beyond the diffraction limit at ~ 1 gigahertz. The near-field plate consists of only capacitive elements and focuses microwaves emanating from a cylindrical source to a spot of size $\approx \lambda/20$ (half-power beamwidth), where λ is the free-space wavelength. These plates will find application in antennas, beam-shaping devices, nonradiative wireless power-transfer systems, microscopy, and lithography.

Since it was first proposed to use sub-wavelength apertures to obtain resolutions beyond the diffraction limit (1), the electromagnetic near field has enjoyed continued scientific interest. Much of the current attention stems

from the work showing that a negative refractive index slab behaves as a perfect lens by focusing both the near- and far-field components emanating from a source (2). Following this work, negative refractive index and negative permittivity (3–6)